California State University San Bernardino School of Computer Science and Engineering

CSE 595D Independent Study <u>Date</u>

June 11, 2019

<u>Time</u>

2:00pm

Place

JB 359

<u>Title</u>

FPGA Design

<u>Student</u>

Jensen Gastelum

<u>Advisor</u>

Dr. Qingquan Sun

Abstract

FPGA's (Field Programmable Gate Array's) are used for their performance. Their performance comes from their unique make of CLBs (Configurable Logic Blocks) which are connected by I/O blocks. To implement a design on a FPGA a user must understand how to program in a HDL (Hardware Description Language) like Verilog. To design a project down to implementation a user must first gain an apprehension of their design then implement it onto a FPGA.